

What is claimed is:

1 1. A method for multi-layer alignment of a
2 semiconductor substrate with alignment marks, comprising:
3 forming a first layer with first alignment marks on the
4 semiconductor substrate, wherein the first
5 alignment marks are separated parallelly by a
6 predetermined distance;
7 forming a second layer with second alignment marks on
8 the first layer, wherein the second alignment marks
9 are separated parallelly by a predetermined
10 distance;
11 measuring the shift distance of each first alignment mark
12 to calculate a first midpoint between the first
13 alignments;
14 measuring the shift distance of each second alignment
15 mark to calculate a second midpoint between the
16 second alignments; and
17 calculating a third midpoint acting as a datum point
18 between the fist midpoint and the second midpoint.

1 2. The method for multi-layer alignment as claimed in
2 claim 1, wherein the second alignment marks and the first
3 alignment marks overlap partially.

1 3. A method for multi-layer alignment for a
2 semiconductor substrate with alignment marks, comprising:
3 forming a first layer with first alignment marks on the
4 semiconductor substrate, wherein the first
5 alignment marks are separated parallelly by a
6 predetermined distance;

7 forming a second layer with second alignment marks on
8 the first layer, wherein the second alignment marks
9 are separated parallelly by a predetermined
10 distance, and the second alignment marks and the
11 first alignment marks are alternately disposed;
12 measuring the shift distance of each first alignment mark
13 to calculate a first midpoint between the first
14 alignments;
15 measuring the shift distance of each second alignment
16 mark to calculate a second midpoint between the
17 second alignments; and
18 calculating a third midpoint acting as a datum point
19 between the fist midpoint and the second midpoint.

1 4. The method for multi-layer alignment as claimed in
2 claim 3, wherein the second alignment marks and the first
3 alignment marks overlap partially.

1 5. A marks for multi-layer alignment of a
2 semiconductor substrate, comprising:
3 a first layer with first alignment marks, wherein the
4 first alignment marks are separated parallelly by
5 a predetermined distance; and
6 a second layer with second alignment marks, wherein the
7 second alignment marks are separated parallelly by
8 a predetermined distance, the second alignment
9 marks and the first alignment marks are alternately
10 disposed, and overlap completely.